Transcend 40-Pin IDE Flash Module (Horizontal)
TS128M ~ 8GDOM40H-S

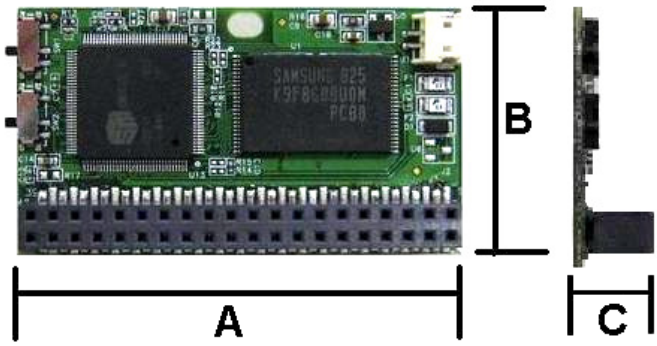
Description

With an IDE interface and strong data retention ability, 40-Pin IDE Flash Modules (Horizontal) are ideal for use in the harsh environments where Industrial PCs, Set-Top Boxes, etc. are used.

Features

- RoHS compliant products
- Storage Capacity: 128MB ~ 8GB
- Operating Voltage: 3.3V ±5% or 5V ±10%
- Operating Temperature: 0℃ ~ 70℃
- Endurance: 2,000,000 Program/Erase cycles
- MTBF: 1,000,000 hours
- Durability of Connector: 10,000 times
- Fully compatible with devices and OS that support the IDE standard (pitch = 2.54mm)
- Built-in ECC function assures high reliability of data transfer
- Supports up to Ultra DMA Mode 4
- Supports Multiword DMA mode 0~4
- Supports PIO Mode 6
- Built-in enhanced wear-leveling algorithm
- Support Security command
- Support S.M.A.R.T (Self-defined)

Placement



Dimensions

Side	Millimeters	Inches
A	55.00 ± 0.15	2.165 ± 0.006
B	30.40 ± 0.15	1.197 ± 0.006
C	9.10 ± 0.20	0.358 ± 0.008

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Pin Assignments

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
01	-RESET	11	HD3	21	DMARQ	31	IREQ
02	GND	12	HD12	22	GND	32	IOIS16B
03	HD7	13	HD2	23	IOWB	33	HA1
04	HD8	14	HD13	24	GND	34	PDIAGB
05	HD6	15	HD1	25	IORB	35	HA0
06	HD9	16	HD14	26	GND	36	HA2
07	HD5	17	HD0	27	IORDY	37	CE1B
08	HD10	18	HD15	28	NC	38	CE2B
09	HD4	19	GND	29	-DMACK	39	DASPB
10	HD11	20	VCC	30	GND	40	GND

Pin Definition

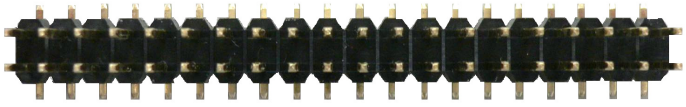
Symbol	Function
HD0 ~ HD15	Data Bus (Bi-directional)
HA0 ~ HA2	Address Bus (Input)
-RESET	Device Reset (Input)
IORB	Device I/O Read (Input)
IOWB	Device I/O Write (Input)
IOIS16B	Transfer Type 8/16 bit (Output)
CE1B, CE2B	Chip Select (Input)
PDIAGB	Pass Diagnostic (Bi-directional)
DASPB	Disk Active/Slave Present (Bi-directional)
DMARQ	DMA request
DMACK-	DMA acknowledge
IREQ	Interrupt Request (Output)
NC	No Connection
GND	Ground
VCC	Vcc Power Input

Input Power

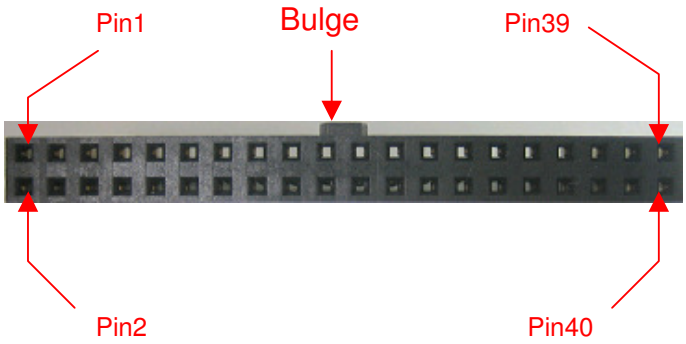
The 40-Pin IDE Flash Module offers 2 ways to get input power, either via the small power cord or through Pin 20 of the IDE connector. If Pin 20 of the IDE connector is defined as NC (No Connect), then the 40-Pin IDE Flash Module must be directly connected to your system's power supply. If Pin 20 of the IDE connector is defined as VCC, then the 40-Pin IDE Flash Module can get necessary power without use of the power cord.

Pin Layout

Male

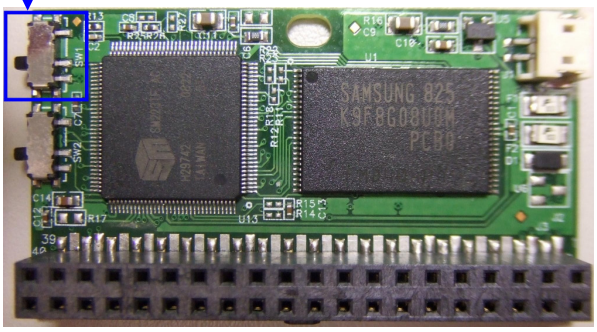


Female

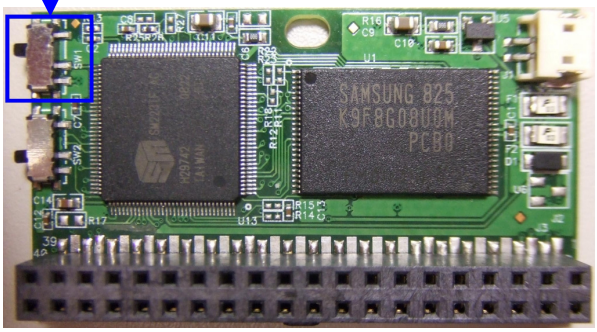


SW1-switch function

Master

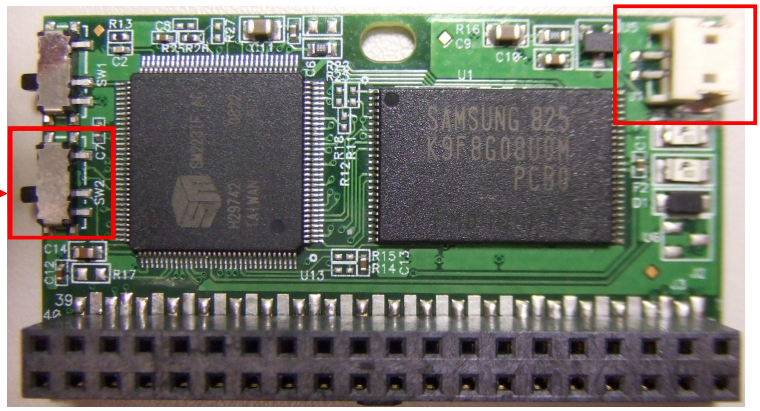


Slave



SW2-switch function and Power connector

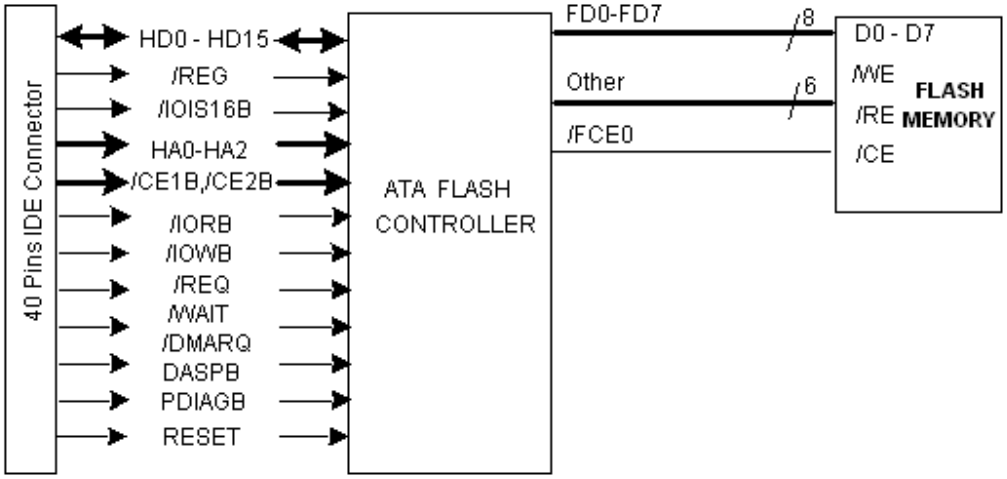
Write-Protect
Disable



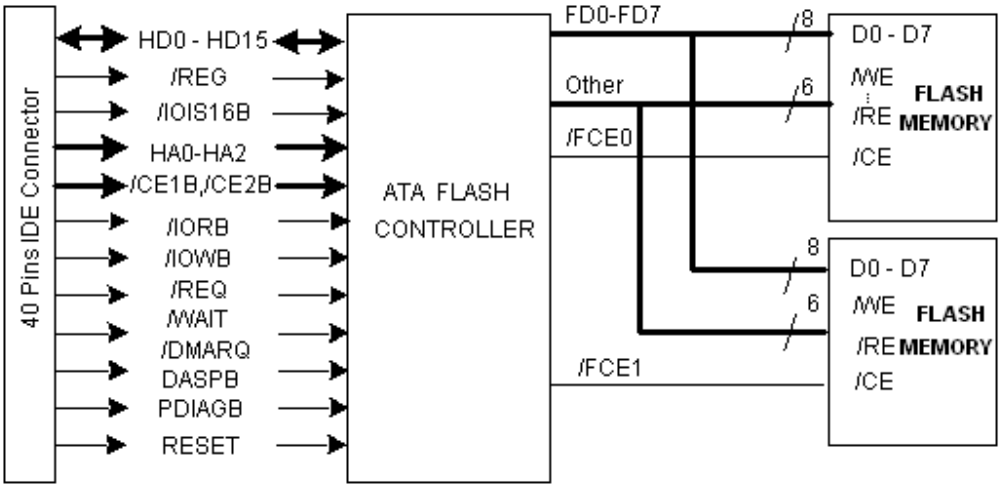
Power connector

Block Diagram

With 1 pcs of Flash Memory:

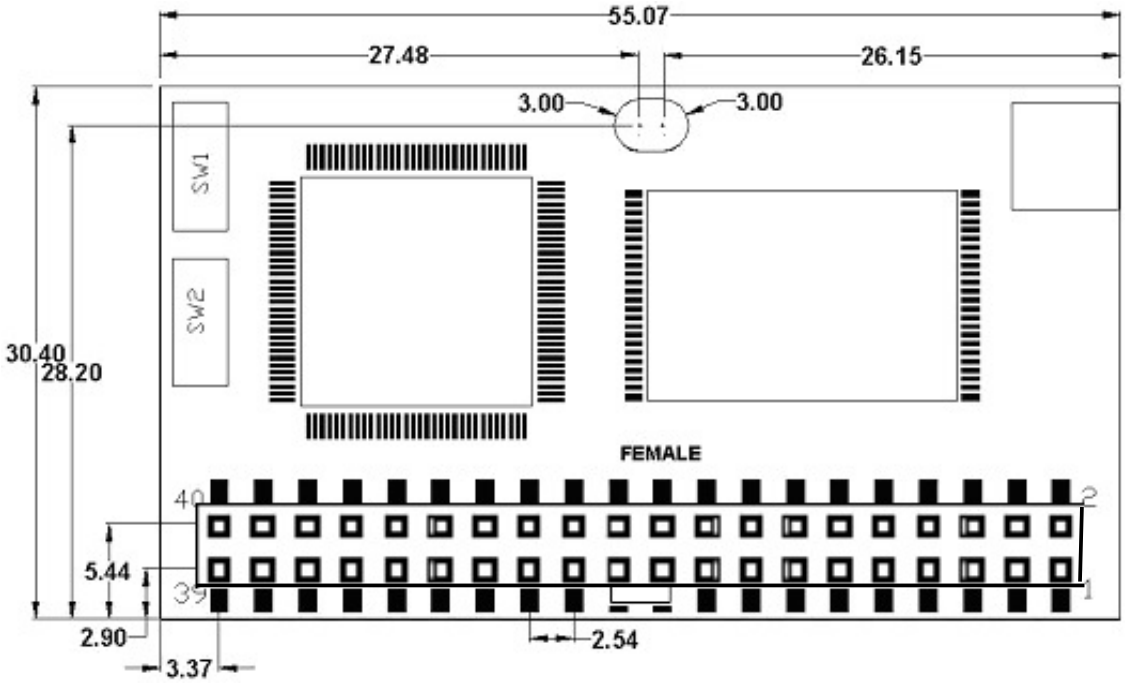


With 2 pcs of Flash Memory:

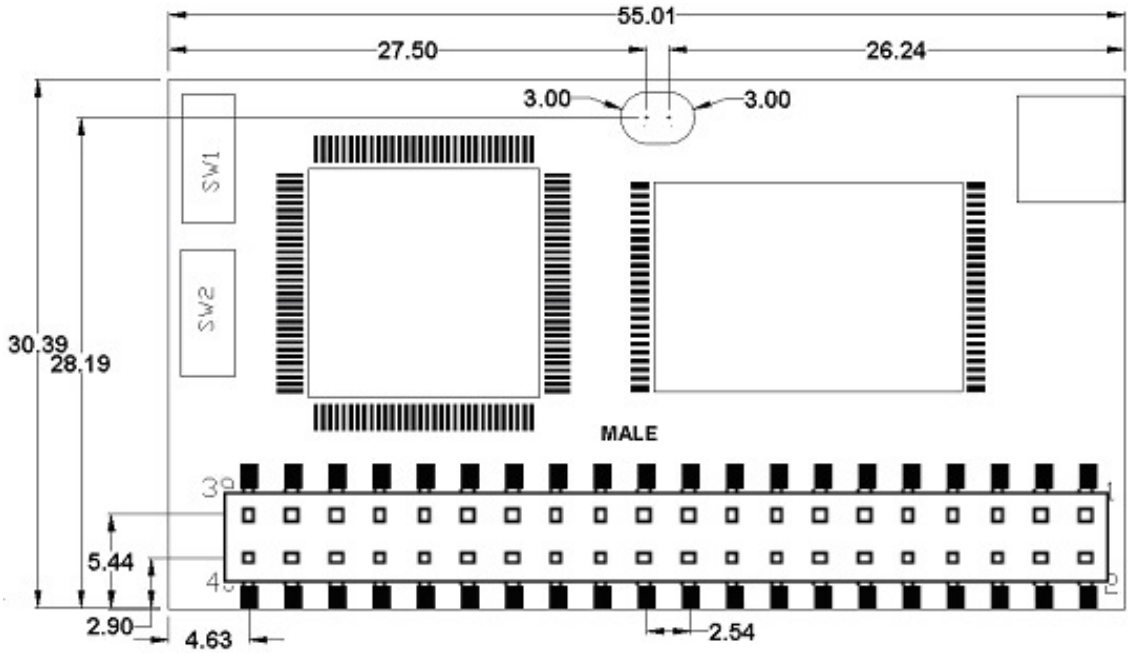


PCB Dimension (unit : mm)

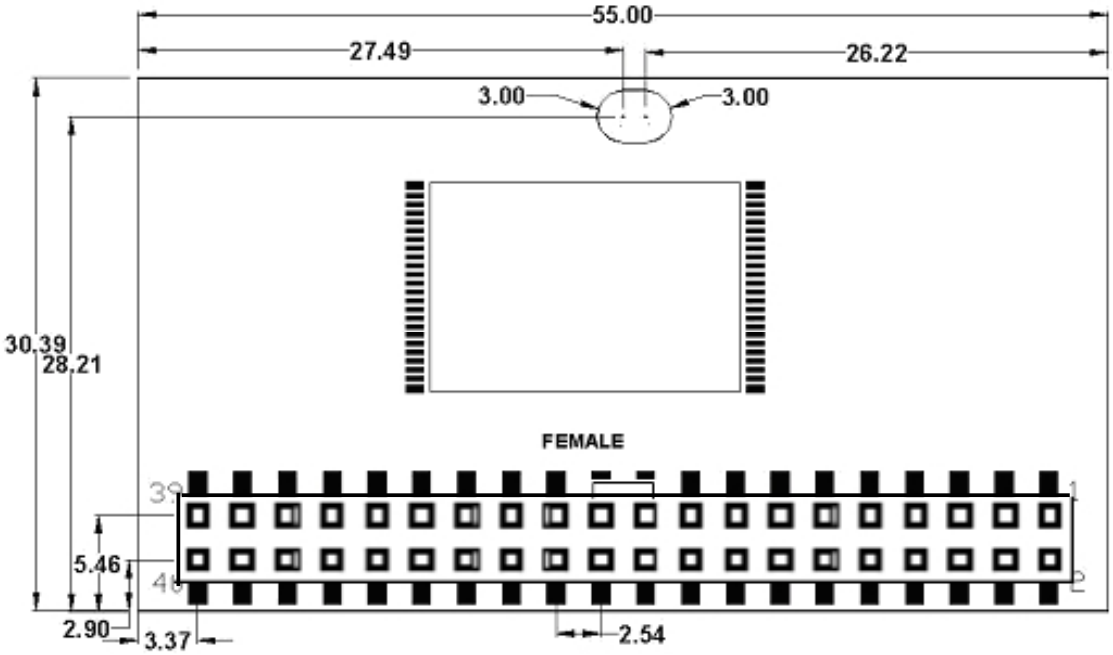
TOP Side IDE 40pin Female (Default)



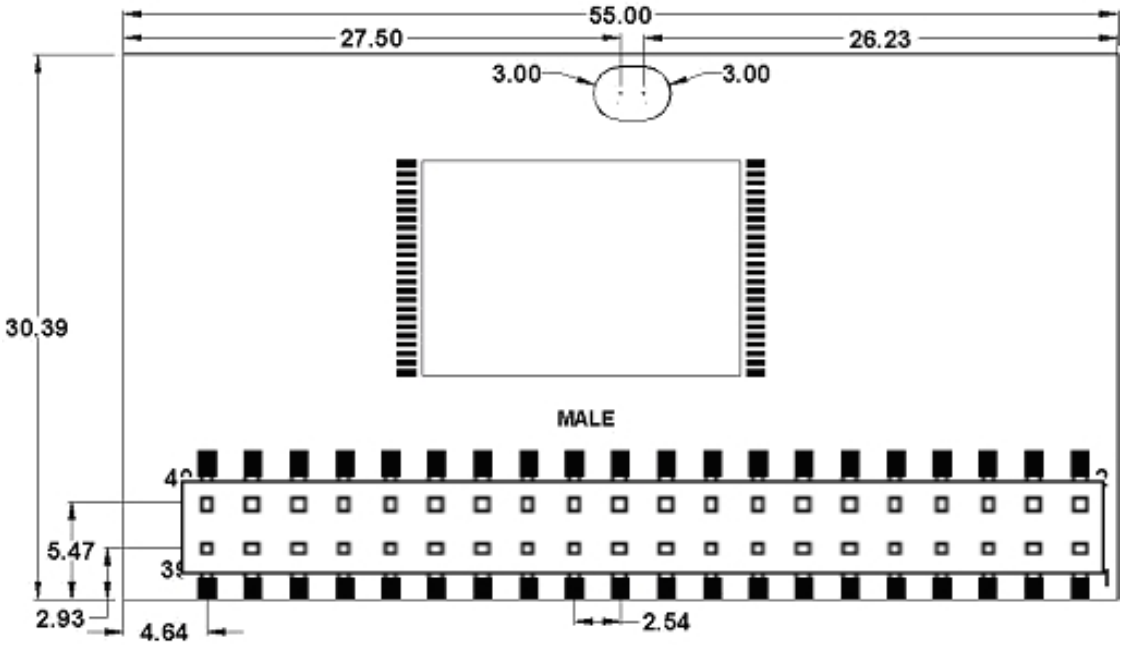
TOP Side IDE 40pin Male



BOT Side IDE 40pin Female



BOT Side IDE 40pin Male



Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDD-VSS	DC Power Supply	-0.6	+6	V
Ta	Operating Temperature	0	+70	°C
Tst	Storage Temperature	-40	+85	°C

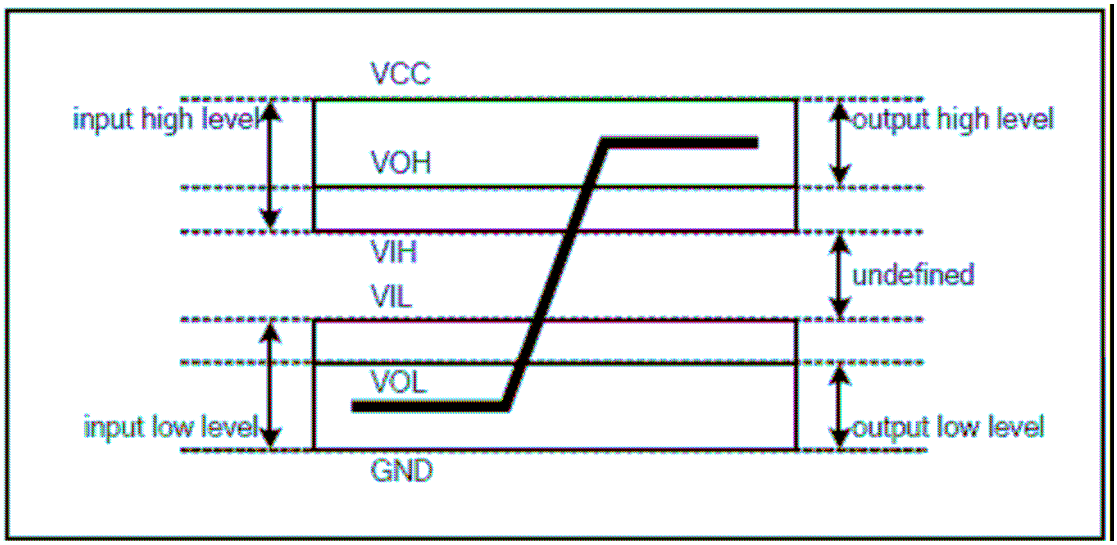
DC Characteristics

(Ta=0 °C to +70 °C, Vcc = 5.0V ±10%)

Parameter	Symbol	Min	Max	Unit	Remark
Supply Voltage	V_{CC}	4.5	5.5	V	
High level output voltage	V_{OH}	V_{CC}-0.8	--	V	
Low level output voltage	V_{OL}	--	0.8	V	
High level input voltage	V_{IH}	4.0	--	V	Non-schmitt trigger
		2.92	--	V	Schmitt trigger[1]
Low level input voltage	V_{IL}	--	0.8	V	Non-schmitt trigger
		--	1.70	V	Schmitt trigger[1]

(Ta=0 °C to +70 °C, Vcc = 3.3V ±5%)

Parameter	Symbol	Min	Max	Unit	Remark
Supply Voltage	V_{CC}	3.135	3.465	V	
High level output voltage	V_{OH}	V_{CC}-0.8	--	V	
Low level output voltage	V_{OL}	--	0.8	V	
High level input voltage	V_{IH}	2.4	--	V	Non-schmitt trigger
		2.05	--	V	Schmitt trigger[1]
Low level input voltage	V_{IL}	--	0.6	V	Non-schmitt trigger
		--	1.25	V	Schmitt trigger[1]


VCC
input high level
VOH
output high level
VIH
undefined
VIL
VOL
input low level
output low level
GND

True IDE PIO Mode Read/Write Timing

	Item	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
t_0	Cycle time (min) [1]	600	383	240	180	120	100	80
t_1	Address Valid to -IORD/-IOWR setup (min)	70	50	30	30	25	15	10
t_2	-IORD/-IOWR (min) [1]	165	125	100	80	70	65	55
t_2	-IORD/-IOWR (min) Register (8 bit)	290	290	290	80	70	65	55
t_{2i}	-IORD/-IOWR recovery time (min)	--	--	--	70	25	25	20
t_3	-IOWR data setup (min)	60	45	30	30	20	20	15
t_4	-IOWR data hold (min)	30	20	15	10	10	5	5
t_5	-IORD data setup (min)	50	35	20	20	20	15	10
t_6	-IORD data hold (min)	5	5	5	5	5	5	5
t_{6Z}	-IORD data tristate (max)[2]	30	30	30	30	30	20	20
t_7	Address valid to IOCS16 assertion (max) [4]	90	50	40	N/A	N/A	N/A	N/A
t_8	Address valid to IOCS16 released (max) [4]	60	45	30	N/A	N/A	N/A	N/A
t_9	-IORD/-IOWR to address valid hold	20	15	10	10	10	10	10
t_{RD}	Read Data Valid to IORDY active (min), if IORDY initially low after tA	0	0	0	0	0	0	0
t_A	IORDY Setup time [3]	35	35	35	35	35	N/A[5]	N/A[5]
t_B	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	N/A[5]	N/A[5]
t_C	IORDY assertion to release (max)	5	5	5	5	5	N/A[5]	N/A[5]

Notes: All timings are in nanoseconds. The maximum load on -IOCS16 is 1 LSTTL with a 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -IORDY high to -IORD high is 0 nsec, but minimum -IORD width shall still be met.

(1) t_0 is the minimum total cycle time, t_2 is the minimum command active time, and t_{2i} is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t_2, and t_{2i} shall be met. The minimum total cycle time requirement is greater than the sum of t_2 and t_{2i}. This means a host implementation can lengthen either or both t_2 or t_{2i} to ensure that t_0 is equal to or greater than the value reported in the device's identify device data.

(2) This parameter specifies the time from the negation edge of -IORD to the time that the data bus is released by the device.

(3) The delay from the activation of -IORD or -IOWR until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle can be completed. If the device is not driving IORDY negated at t_A after the activation of -IORD or -IOWR, then t_5 shall be met and t_{RD} is not applicable. If the device is driving IORDY negated at the time t_A after the activation of -IORD or -IOWR, then t_{RD} shall be met and t5 is not applicable.

(4) t_7 and t_8 apply only to modes 0, 1 and 2. For other modes, this signal is not valid.

(5) IORDY is not supported in this mode.

True IDE PIO Mode Timing Diagram

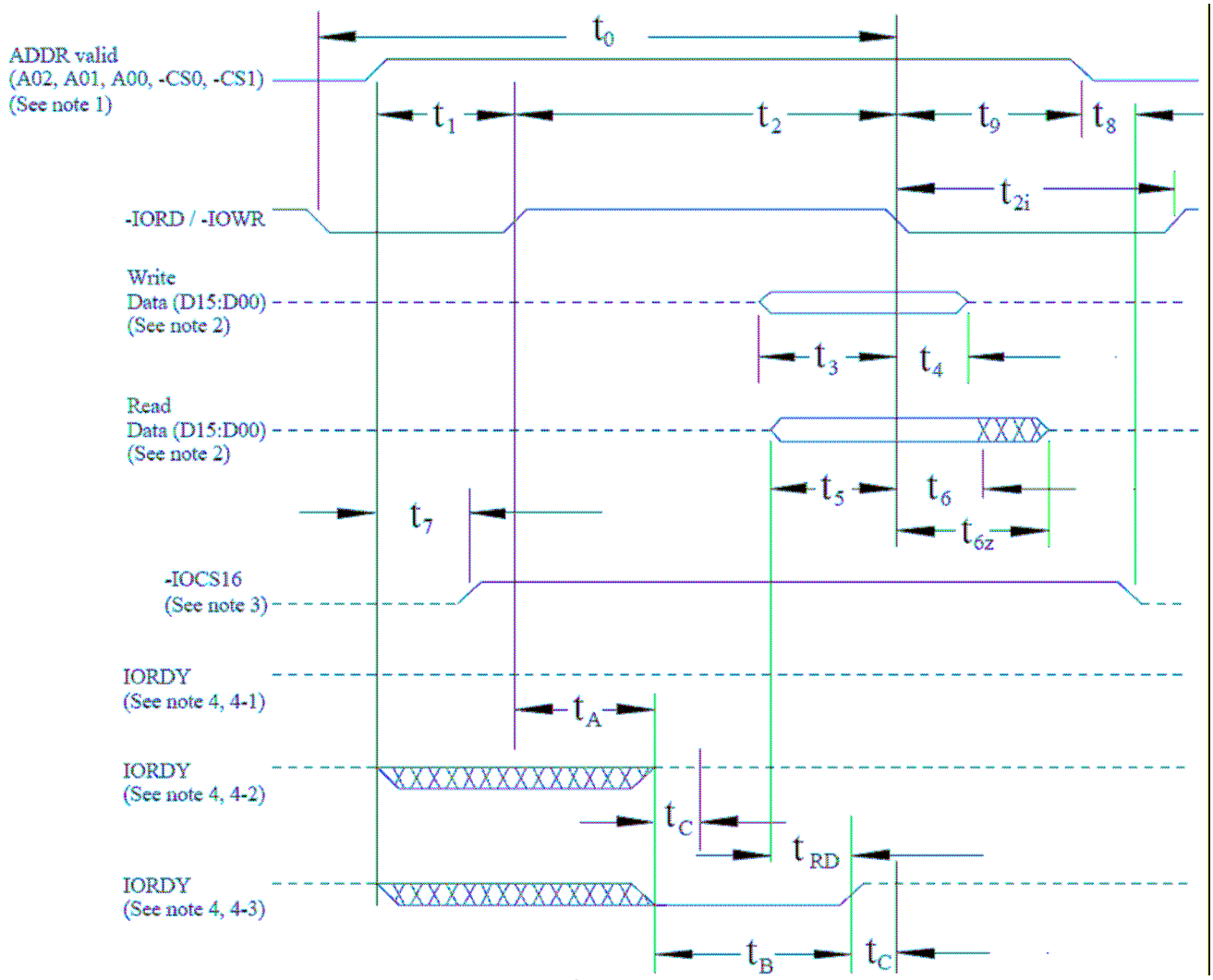


Figure 1: True IDE PIO Mode Timing Diagram

Notes:
(1) Device address consists of -CS0, -CS1, and A[02::00]
(2) Data consists of D[15::00] (16-bit) or D[07::00] (8 bit)
(3) -IOCS16 is shown for PIO modes 0, 1 and 2. For other modes, this signal is ignored.
(4) The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after t_A from the assertion of -IORD or -IOWR. The assertion and negation of IORDY is described in the following three cases:
(4-1) Device never negates IORDY: No wait is generated.
(4-2) Device starts to drive IORDY low before t_A, but causes IORDY to be asserted before t_A: No wait generated.
(4-3) Device drives IORDY low before t_A: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and -IORD is asserted, the device shall place read data on D15-D00 for t_{RD} before causing IORDY to be asserted.

True IDE Multiword DMA Mode Read/Write Timing Specification

	Item	Mode 0 (ns)	Mode 1 (ns)	Mode 2 (ns)	Mode 3 (ns)	Mode 4 (ns)
t_0	Cycle time (min) [1]	480	150	120	100	80
t_D	-IORD / -IOWR asserted width(min) [1]	215	80	70	65	55
t_E	-IORD data access (max)	150	60	50	50	45
t_F	-IORD data hold (min)	5	5	5	5	5
t_G	-IORD/-IOWR data setup (min)	100	30	20	15	10
t_H	-IOWR data hold (min)	20	15	10	5	5
t_I	DMACK to –IORD/-IOWR setup (min)	0	0	0	0	0
t_J	-IORD / -IOWR to -DMACK hold (min)	20	5	5	5	5
t_{KR}	-IORD negated width (min) [1]	50	50	25	25	20
t_{KW}	-IOWR negated width (min) [1]	215	50	25	25	20
t_{LR}	-IORD to DMARQ delay (max)	120	40	35	35	35
t_{LW}	-IOWR to DMARQ delay (max)	40	40	35	35	35
t_M	CS(1:0) valid to –IORD / -IOWR	50	30	25	10	5
t_N	CS(1:0) hold	15	10	10	10	10
t_Z	-DMACK	20	25	25	25	25

Notes:

(1) t_0 is the minimum total cycle time and t_D is the minimum command active time, while t_{KR} and t_{KW} are the minimum command recovery time or command inactive time for input and output cycles respectively. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t_0, t_D, t_{KR}, and t_{KW} shall be met. The minimum total cycle time requirement is greater than the sum of t_D and t_{KR} or t_{KW}.for input and output cycles respectively. This means a host implementation can lengthen either or both of t_D and either of t_{KR}, and t_{KW} as needed to ensure that t_0 is equal to or greater than the value reported in the device's identify device data.

True IDE Multiword DMA Mode Read/Write Timing Diagram

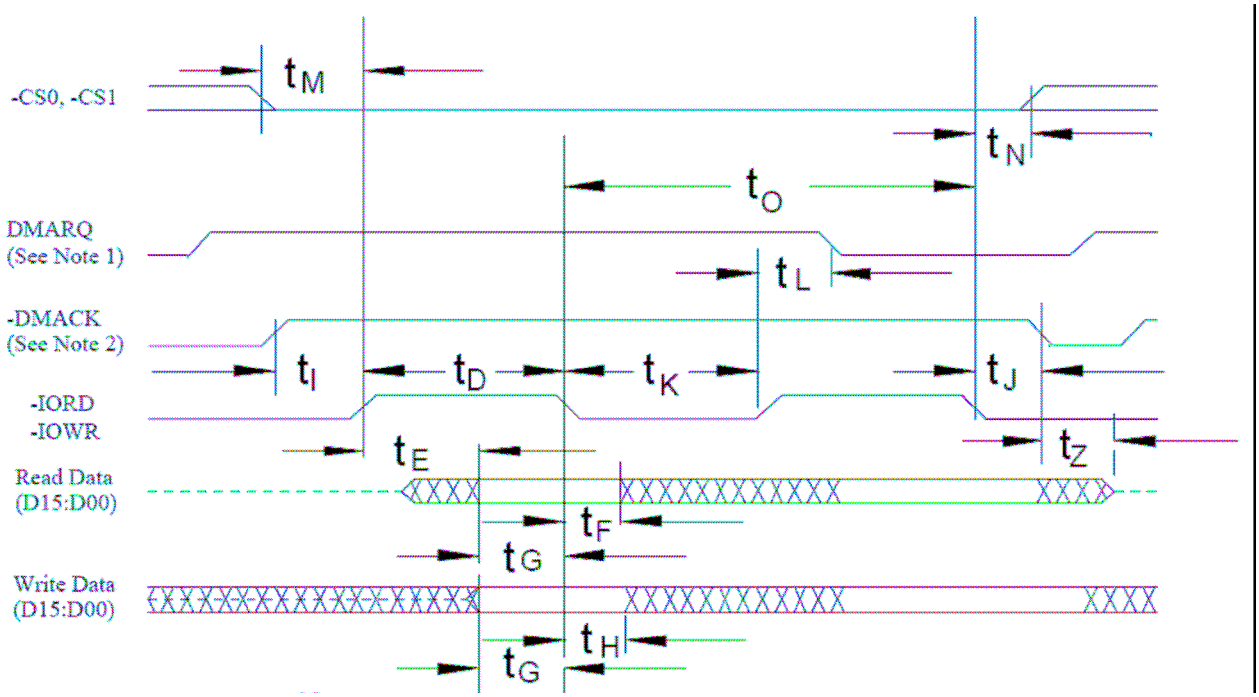


Figure 2: True IDE Multiword DMA Mode Read/Write Timing Diagram

Notes:
(1) If the Card cannot sustain continuous, minimum cycle time DMA transfers, it may negate DMARQ within the time specified from the start of a DMA transfer cycle to suspend the DMA transfers in progress and reassert the signal at a later time to continue the DMA operation.
(2) This signal may be negated by the host to suspend the DMA transfer in progress.

Ultra DMA Mode Read/Write Timing Specification

Ultra DMA is an optional data transfer protocol used with the READ DMA, and WRITE DMA, commands. When this protocol is enabled, the Ultra DMA protocol shall be used instead of the Multiword DMA protocol when these commands are issued by the host. This protocol applies to the Ultra DMA data burst only. When this protocol is used there are no changes to other elements of the ATA protocol.

UDMA Signal	Type	TRUE IDE MODE UDMA
DMARQ	Output	DMARQ
DMACK	Input	-DMACK
STOP	Input	STOP[1]
HDMARDY(R) HSTROBE(W)	Input	-HDMARDY[1,2] HSTROBE(W)[1,3,4]
DDMARDY(W) DSTROBE(R)	Output	-DDMARDY(W)[1,3] DSTROBE(R)[1,2,4]
DATA	Bidir	D[15:00]
ADDRESS	Input	A[02:00][5]
CSEL	input	-CSEL
INTRQ	Output	INTRQ
Card Select	Input	-CS0 -CS1

Notes: 1) The UDMA interpretation of this signal is valid only during an Ultra DMA data burst.
2) The UDMA interpretation of this signal is valid only during and Ultra DMA data burst during a DMA Read command.
3) The UDMA interpretation of this signal is valid only during an Ultra DMA data burst during a DMA Write command.
4) The HSTROBE and DSTROBE signals are active on both the rising and the falling edge.
5) Address lines 03 through 10 are not used in True IDE mode.

Several signal lines are redefined to provide different functions during an Ultra DMA data burst. These lines assume their UDMA definitions when:

1. an Ultra DMA mode is selected, and

2. a host issues a READ DMA, or a WRITE DMA command requiring data transfer, and

3. the device asserts (-)DMARQ, and

4. the host asserts (-)DMACK.

These signal lines revert back to the definitions used for non-Ultra DMA transfers upon the negation of -DMACK by the host at the termination of an Ultra DMA data burst.

With the Ultra DMA protocol, the STROBE signal that latches data from D[15:00] is generated by the

same agent (either host or device) that drives the data onto the bus. Ownership of D[15:00] and this data strobe signal are given either to the device during an Ultra DMA data-in burst or to the host for an Ultra DMA data-out burst.

During an Ultra DMA data burst a sender shall always drive data onto the bus, and, after a sufficient time to allow for propagation delay, cable settling, and setup time, the sender shall generate a STROBE edge to latch the data. Both edges of STROBE are used for data transfers so that the frequency of STROBE is limited to the same frequency as the data.

Words in the IDENTIFY DEVICE data indicate support of the Ultra DMA feature and the Ultra DMA modes the device is capable of supporting. The Set transfer mode subcommand in the SET FEATURES command shall be used by a host to select the Ultra DMA mode at which the system operates. The Ultra DMA mode selected by a host shall be less than or equal to the fastest mode of which the device is capable. Only one Ultra DMA mode shall be selected at any given time. All timing requirements for a selected Ultra DMA mode shall be satisfied. Devices supporting any Ultra DMA mode shall also support all slower Ultra DMA modes.

An Ultra DMA capable device shall retain the previously selected Ultra DMA mode after executing a software reset sequence or the sequence caused by receipt of a DEVICE RESET command if a SET FEATURES disable reverting to defaults command has been issued. The device may revert to a Multiword DMA mode if a SET FEATURES enable reverting to default has been issued. An Ultra DMA capable device shall clear any previously selected Ultra DMA mode and revert to the default non-Ultra DMA modes after executing a power-on or hardware reset.

Both the host and device perform a CRC function during an Ultra DMA data burst. At the end of an Ultra DMA data burst the host sends its CRC data to the device. The device compares its CRC data to the data sent from the host. If the two values do not match, the device reports an error in the error register. If an error occurs during one or more Ultra DMA data bursts for any one command, the device shall report the first error that occurred. If the device detects that a CRC error has occurred before data transfer for the command is complete, the device may complete the transfer and report the error or abort the command and report the error.

NOTE – If a data transfer is terminated before completion, the assertion of INTRQ should be passed through to the host software driver regardless of whether all data requested by the command has been transferred.

Ultra DMA Data Burst Timing Requirements

Name	UDMA Mode 0		UDMA Mode 1		UDMA Mode 2		UDMA Mode 3		UDMA Mode 4		Measure location (See Note 2)
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{2CYCTYP}$	240		160		120		90		60		Sender
t_{CYC}	112		73		54		39		25		Note 3
t_{2CYC}	230		153		115		86		57		Sender
t_{DS}	15.0		10.0		7.0		7.0		5.0		Recipient
t_{DH}	5.0		5.0		5.0		5.0		5.0		Recipient
t_{DVS}	70.0		48.0		31.0		20.0		6.7		Sender
t_{DVH}	6.2		6.2		6.2		6.2		6.2		Sender
t_{CS}	15.0		10.0		7.0		7.0		5.0		Device
t_{CH}	5.0		5.0		5.0		5.0		5.0		Device
t_{CVS}	70.0		48.0		31.0		20.0		6.7		Host
t_{CVH}	6.2		6.2		6.2		6.2		6.2		Host
t_{ZFS}	0		0		0		0		0		Device
t_{DZFS}	70.0		48.0		31.0		20.0		6.7		Sender
t_{FS}		230		200		170		130		120	Device
t_{LI}	0	150	0	150	0	150	0	100	0	100	Note 4
t_{MLI}	20		20		20		20		20		Host
t_{UI}	0		0		0		0		0		Host
t_{AZ}		10		10		10		10		10	Note 5
t_{ZAH}	20		20		20		20		20		Host
t_{ZAD}	0		0		0		0		0		Device
t_{ENV}	20	70	20	70	20	70	20	55	20	55	Host
t_{RFS}		75		70		60		60		60	Sender
t_{RP}	160		125		100		100		100		Recipient
t_{IORDYZ}		20		20		20		20		20	Device
t_{ZIORDY}	0		0		0		0		0		Device
t_{ACK}	20		20		20		20		20		Host
t_{SS}	50		50		50		50		50		Sender

Notes: All Timings in ns

(1) All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.

(2) All signal transitions for a timing parameter shall be measured at the connector specified in the measurement location column. For example, in the case of t_{RFS}, both STROBE and -DMARDY transitions are measured at the sender connector.

(3) The parameter t_{CYC} shall be measured at the recipient's connector farthest from the sender.

(4) The parameter t_{LI} shall be measured at the connector of the sender or recipient that is responding to an incoming transition from the recipient or sender respectively. Both the incoming signal and the outgoing response shall be measured at the same connector.

(5) The parameter t_{AZ} shall be measured at the connector of the sender or recipient that is driving the bus but must release the bus to allow for a bus turnaround.

(6) See Page 14 the AC Timing requirements in Ultra DMA AC Signal Requirements.

Ultra DMA Data Burst Timing Descriptions

Name	Comment	Notes
$t_{2CYCTYP}$	Typical sustained average two cycle time	
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	
t_{DS}	Data setup time at recipient (from data valid until STROBE edge)	2,
t_{DH}	Data hold time at recipient (from STROBE edge until data may become invalid)	2,
t_{DVS}	Data valid setup time at sender (from data valid until STROBE edge)	3
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)	3
t_{CS}	CRC word setup time at device	2
t_{CH}	CRC word hold time device	2
t_{CVS}	CRC word valid setup time at host (from CRC valid until -DMACK negation)	3
t_{CVH}	CRC word valid hold time at sender (from -DMACK negation until CRC may become invalid)	3
t_{ZFS}	Time from STROBE output released-to-driving until the first transition of critical timing.	
t_{DZFS}	Time from data output released-to-driving until the first transition of critical timing.	
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	
t_{LI}	Limited interlock time	1
t_{MLI}	Interlock time with minimum	1
t_{UI}	Unlimited interlock time	1
t_{AZ}	Maximum time allowed for output drivers to release (from asserted or negated)	
t_{ZAH}	Minimum delay time required for output	
t_{ZAD}	drivers to assert or negate (from released)	
t_{ENV}	Envelope time (from -DMACK to STOP and -HDMARDY during data in burst initiation and from DMACK to STOP during data out burst initiation)	
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of -DMARDY)	
t_{RP}	Ready-to-pause time (that recipient shall wait to pause after negating -DMARDY)	
t_{IORDYZ}	Maximum time before releasing IORDY	
t_{ZIORDY}	Minimum time before driving IORDY	4,
t_{ACK}	Setup and hold times for -DMACK (before assertion or negation)	
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	

Notes:

(1) The parameters t_{UI}, t_{MLI} (in Page 19: Ultra DMA Data-In Burst Device Termination Timing and Page 20: Ultra DMA Data-In Burst Host Termination Timing), and t_{LI} indicate sender-to-recipient or recipient-to-sender interlocks,i.e., one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding.t_{UI} is an unlimited interlock that has no maximum time value. t_{ML}I is a limited time-out that has a defined minimum. t_{LI} is a limited time-out that has a defined maximum.

(2) 80-conductor cabling (see see ATA specification :Annex A)) shall be required in order to meet setup (t_{DS}, t_{CS}) and hold (t_{DH}, t_{CH}) times in modes greater than 2.

(3) Timing for t_{DVS}, t_{DVH}, t_{CVS} and t_{CVH} shall be met for lumped capacitive loads of 15 and 40 pF at the connector where the Data and STROBE signals have the same capacitive load value. Due to reflections on the cable, these timing measurements are not valid in a normally functioning system.

(4) For all timing modes the parameter t_{ZIORDY} may be greater than t_{ENV} due to the fact that the host has a pull-up on IORDY-

giving it a known state when released.

Ultra DMA Sender and Recipient IC Timing Requirements

Name	UDMA Mode 0 (ns)		UDMA Mode 1 (ns)		UDMA Mode 2 (ns)		UDMA Mode 3 (ns)		UDMA Mode 4 (ns)	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{DSIC}	14.7		9.7		6.8		6.8		4.8	
t_{DHIC}	4.8		4.8		4.8		4.8		4.8	
t_{DVSIC}	72.9		50.9		33.9		22.6		9.5	
t_{DVHIC}	9.0		9.0		9.0		9.0		9.0	
t_{DSIC}	Recipient IC data setup time (from data valid until STROBE edge) (see note 2)									
t_{DHIC}	Recipient IC data hold time (from STROBE edge until data may become invalid) (see note 2)									
t_{DVSIC}	Sender IC data valid setup time (from data valid until STROBE edge) (see note 3)									
t_{DVHIC}	Sender IC data valid hold time (from STROBE edge until data may become invalid) (see note 3)									

Notes:
(1) All timing measurement switching points(low to high and high to low) shall be taken at 1.5 V.
(2) The correct data value shall be captured by the recipient given input data with a slew rate of 0.4 V/ns rising and falling and the input STROBE with a slew rate of 0.4 V/ns rising and falling at t_{DSIC} and t_{DHIC} timing (as measured through 1.5 V).
(3) The parameters t_{DVSIC} and t_{DVHIC} shall be met for lumped capacitive loads of 15 and 40 pF at the IC where all signals have the same capacitive load value. Noise that may couple onto the output signals from external sources has not been included in these values.

Ultra DMA AC Signal Requirements

Name	**Comment**	**Min[V/ns]**	**Max [V/ns]**	Note
S_{RISE}	Rising Edge Slew Rate for any signal		1.25	1
S_{FALL}	Falling Edge Slew Rate for any signal		1.25	1

Note:
(1) The sender shall be tested while driving an 18 inch long, 80 conductor cable with PVC insulation material. The signal under test shall be cut at a test point so that it has not trace, cable or recipient loading after the test point. All other signals should remain connected through to the recipient. The test point may be located at any point between the sender's series termination resistor and one half inch or less of conductor exiting the connector. If the test point is on a cable conductor rather than the PCB, an adjacent ground conductor shall also be cut within one half inch of the connector.

The test load and test points should then be soldered directly to the exposed source side connectors. The test loads consist of a 15 pF or a 40 pF, 5%, 0.08 inch by 0.05 inch surface mount or smaller size capacitor from the test point to ground. Slew rates shall be met for both capacitor values.

Measurements shall be taken at the test point using a <1 pF, >100 Kohm, 1 Ghz or faster probe and a 500 MHz or faster oscilloscope. The average rate shall be measured from 20% to 80% of the settled VOH level with data transitions at least 120 nsec apart. The settled VOH level shall be measured as the average output

high level under the defined testing conditions from 100 nsec after 80% of a rising edge until 20% of the subsequent falling edge.

Initiating an Ultra DMA Data-In Burst

(a) An Ultra DMA Data-In burst is initiated by following the steps lettered below. The timing diagram is shown in below: Ultra DMA Data-In Burst Initiation Timing. The associated timing parameters are specified in Page 12: Ultra DMA Data Burst Timing Requirements and are described in Page 13: Ultra DMA Data Burst Timing Descriptions.

(b) The following steps shall occur in the order they are listed unless otherwise specifically allowed:

(c) The host shall keep -DMACK in the negated state before an Ultra DMA data burst is initiated.

(d) The device shall assert DMARQ to initiate an Ultra DMA data burst. After assertion of DMARQ the device shall not negate DMARQ until after the first negation of DSTROBE.

(e) Steps (c), (d), and (e) may occur in any order or at the same time. The host shall assert STOP.

(f) The host shall negate -HDMARDY.

(g) In True IDE mode, the host shall not assert -CS0, -CS1 and A[02:00].

(h) Steps (c), (d), and (e) shall have occurred at least t_{ACK} before the host asserts -DMACK. The host shall keep -DMACK asserted until the end of an Ultra DMA data burst.

(i) The host shall release D[15:00] within t_{AZ} after asserting -DMACK.

(j) The device may assert DSTROBE t_{ZIORDY} after the host has asserted -DMACK. While operating in True IDE mode, once the device has driven DSTROBE, the device shall not release DSTROBE until after the host has negated -DMACK at the end of an Ultra DMA data burst.

(k) The host shall negate STOP and assert -HDMARDY within t_{ENV} after asserting -DMACK. After negating STOP and asserting -HDMARDY, the host shall not change the state of either signal until after receiving the first transition of DSTROBE from the device (i.e., after the first data word has been received).

(l) The device shall drive D[15:00] no sooner than t_{ZAD} after the host has asserted -DMACK, negated STOP, and asserted -HDMARDY.

(m) The device shall drive the first word of the data transfer onto D[15:00]. This step may occur when the device first drives D[15:00] in step (j).

(n) To transfer the first word of data the device shall negate DSTROBE within t_{FS} after the host has negated STOP and asserted -HDMARDY. The device shall negate DSTROBE no sooner than t_{DVS} after driving the first word of data onto D[15:00].