

TS256MQR72V6UL

240PIN DDR2 667 VLP Registered DIMM
2048MB With 128Mx8 CL5

Description

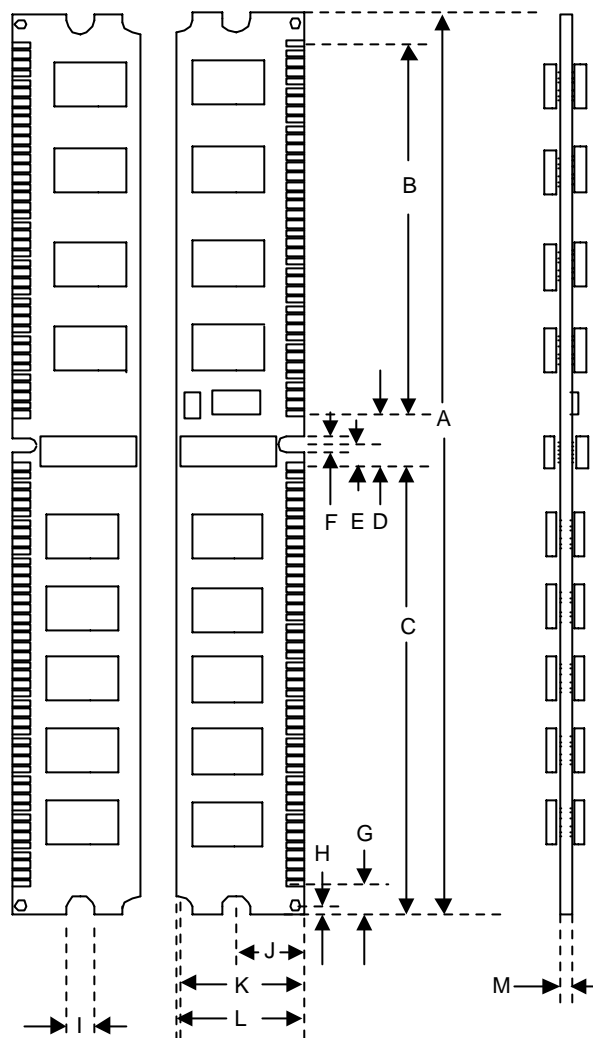
The TS256MQR72V6U is a 256M x 72bits DDR2-667 Registered DIMM. The TS256MQR72V6UL consists of 18 pcs 128Mx8 bits DDR2 SDRAMs in 68 ball FBGA package, 2 pcs register in 96 ball uBGA package, 1 pcs PLL driver IC and a 2048 bits serial EEPROM on a 240-pin printed circuit board. The TS256MQR72V6UL is a Dual In-Line Memory Module and is intended for mounting into 240-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

- RoHS compliant products.
- JEDEC standard 1.8V \pm 0.1V Power supply
- VDDQ=1.8V \pm 0.1V
- Max clock Freq: 333MHZ; 667Mb/S/Pin.
- Posted CAS
- Programmable CAS Latency: 3,4,5
- Programmable Additive Latency :0, 1,2,3 and 4
- Write Latency (WL) = Read Latency (RL)-1
- Burst Length: 4,8(Interleave/nibble sequential)
- Programmable sequential / Interleave Burst Mode
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- Off-Chip Driver (OCD) Impedance Adjustment
- MRS cycle with address key programs.
- On Die Termination
- Serial presence detect with EEPROM

Placement



09-3050

TS256MQR72V6UL

240PIN DDR2 667 VLP Registered DIMM
2048MB With 128Mx8 CL5

Dimensions

Side	Millimeters	Inches
A	133.35 ±0.15	5.250 ±0.006
B	55	2.165
C	63	2.480000
D	5	0.197
E	2.5	0.0980
F	1.5 ±0.10	0.059 ±0.039
G	5.175	0.204
H	2.2	0.867
I	4	0.157
J	10	0.394
K	17.8	0.701
L	18.3 ±0.15	0.72 ±0.006
M	1.27 ±0.10	0.050 ±0.004

(Refer Placement)

Pin Description

Symbol	Function
A0~A13, BA0,~BA2	Address input, bank address
DQ0~DQ63	Data Input / Output.
CB0~CB7	Data Check Bits Input/Output
DQS0~DQS8	Data strobe
/DQS0~/DQS8	Data strobe , negative line
CK0, /CK0	Clock Input.
CKE0, CKE1	Clock Enable Input.
ODT0, ODT1	On-die termination control line
/CS0, /CS1	Chip Select Input.
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
DM0~DM8	Data-in Mask
/DQS9~/DQS17	Data strobes(Read),negative line
VDD	+1.8 Voltage power supply
VDDQ	+1.8 Voltage Power Supply for DQS
VREF	Power Supply for Reference
VDDSPD	Serial EEPROM Positive Power Supply
SA0~SA2	Address select for EEPROM
SCL	Serial PD Clock
SDA	Serial PD Add/Data input/output
VSS	Ground
/RESET	Register and PLL control pin
/Err_Out	Parity error found in the bus
Par_In	Parity bit for address and control bus
NC	No Connection

TS256MQR72V6UL

240PIN DDR2 667 VLP Registered DIMM

2048MB With 128Mx8 CL5

Pinouts:

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
01	VREF	41	VSS	81	DQ33	121	VSS	161	CB4
02	VSS	42	CB0	82	VSS	122	DQ4	162	CB5
03	DQ0	43	CB1	83	/DQS4	123	DQ5	163	VSS
04	DQ1	44	VSS	84	DQS4	124	VSS	164	DM8,DQS17
05	VSS	45	/DQS8	85	VSS	125	DM0,DQS9	165	NC,/DQS17
06	/DQS0	46	DQS8	86	DQ34	126	NC,/DQS9	166	VSS
07	DQS0	47	VSS	87	DQ35	127	VSS	167	CB6
08	VSS	48	CB2	88	VSS	128	DQ6	168	CB7
09	DQ2	49	CB3	89	DQ40	129	DQ7	169	VSS
10	DQ3	50	VSS	90	DQ41	130	VSS	170	VDDQ
11	VSS	51	VDDQ	91	VSS	131	DQ12	171	NC, **CKE1
12	DQ8	52	CKE0	92	/DQS5	132	DQ13	172	VDD
13	DQ9	53	VDD	93	DQS5	133	VSS	173	NC
14	VSS	54	NC, BA2	94	VSS	134	DM1,DQS10	174	NC
15	/DQS1	55	NC, ***Err_Out	95	DQ42	135	NC,/DQS10	175	VDDQ
16	DQS1	56	VDDQ	96	DQ43	136	VSS	176	A12
17	VSS	57	A11	97	VSS	137	*RFU	177	A9
18	/RESET	58	A7	98	DQ48	138	*RFU	178	VDD
19	NC	59	VDD	99	DQ49	139	VSS	179	A8
20	VSS	60	A5	100	VSS	140	DQ14	180	A6
21	DQ10	61	A4	101	SA2	141	DQ15	181	VDDQ
22	DQ11	62	VDDQ	102	NC	142	VSS	182	A3
23	VSS	63	A2	103	VSS	143	DQ20	183	A1
24	DQ16	64	VDD	104	/DQS6	144	DQ21	184	VDD
25	DQ17	65	VSS	105	DQS6	145	VSS	185	CK0
26	VSS	66	VSS	106	VSS	146	DM2,DQS11	186	/CK0
27	/DQS2	67	VDD	107	DQ50	147	NC,/DQS11	187	VDD
28	DQS2	68	NC, ***Par_in	108	DQ51	148	VSS	188	A0
29	VSS	69	VDD	109	VSS	149	DQ22	189	VDD
30	DQ18	70	A10/AP	110	DQ56	150	DQ23	190	BA1
31	DQ19	71	BA0	111	DQ57	151	VSS	191	VDDQ
32	VSS	72	VDDQ	112	VSS	152	DQ28	192	/RAS
33	DQ24	73	/WE	113	/DQS7	153	DQ29	193	/CS0
34	DQ25	74	/CAS	114	DQS7	154	VSS	194	VDDQ
35	VSS	75	VDDQ	115	VSS	155	DM3,DQS12	195	ODT0
36	/DQS3	76	NC, **/CS1	116	DQ58	156	NC,/DQS12	196	A13
37	DQS3	77	ODT1	117	DQ59	157	VSS	197	VDD
38	VSS	78	VDDQ	118	VSS	158	DQ30	198	VSS
39	DQ26	79	VSS	119	SDA	159	DQ31	199	DQ36
40	DQ27	80	DQ32	120	SCL	160	VSS	200	DQ37
								201	VSS
								202	DM4,DQS13
								203	NC,/DQS13
								204	VSS
								205	DQ38
								206	DQ39
								207	VSS
								208	DQ44
								209	DQ45
								210	VSS
								211	DM5,DQS14
								212	NC,/DQS14
								213	VSS
								214	DQ46
								215	DQ47
								216	VSS
								217	DQ52
								218	DQ53
								219	VSS
								220	*RFU
								221	*RFU
								222	VSS
								223	DM6,DQS15
								224	NC,/DQS15
								225	VSS
								226	DQ54
								227	DQ55
								228	VSS
								229	DQ60
								230	DQ61
								231	VSS
								232	DM7,DQS16
								233	NC,/DQS16
								234	VSS
								235	DQ62
								236	DQ63
								237	VSS
								238	VDDSPD
								239	SA0
								240	SA1

*RFU = Reserved for Future Use

**CKE1, /CS1 are used for 2 rank registered DIMM.

***NC, /Err Out and NC, /Par_In are for optional function to check address and command parity.